REMARKS

Claim 8 has been amended. No new matter has been added.

The Rejections under 35 U.S.C. § 103(a)

Claims 1-8 and 10-17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of U.S. Patent Application Publication No. 2002/0057247 to *Lee et al.* ("*Lee*"), U.S. Patent No. 6,753,855 to *Yu* ("*Yu*"), U.S. Patent Application Publication No. 2004/0008176 to *Nuimura* ("*Nuimura*"), and U.S. Patent Application Publication No. 2002/0130830 to *Park* ("*Park*"). Applicant respectfully traverses, noting that none of these references, singly or in combination, discloses every element of any of these claims as amended. More specifically, none discloses an inverter control unit for selectively outputting a timing signal according to the control signal from the mode setting unit. Also, none discloses an inverter that can operate in both synchronous and asynchronous mode. Additionally, none discloses the operation in synchronous or asynchronous mode depending upon whether a timing signal is received. Finally, under the latest Office Action's interpretation of *Nuimura*, *Nuimura* would teach away from Applicants' claims.

First, no reference discloses or suggests an inverter control unit for selectively outputting a timing signal according to a control signal from a mode setting unit. The latest Office Action asserts that first switching unit 510 and second switching unit 520 of *Lee* correspond to Applicants' claimed "inverter control unit" and "mode setting unit," respectively. However, the only output of second switching unit 520 disclosed in *Lee* is either a common electrode voltage or an external bias voltage, and these voltages are both output to a common electrode line of LCD panel 600, not to first switching unit 510 (¶ [0119]). Thus, even if the second switching unit 520 of *Lee* can be considered a "mode setting unit," this mode setting unit does not output any signals to first switching unit 510, or an "inverter control unit." Rather, it only outputs signals to an LCD panel 600 (Id.). Additionally, any output of such a mode setting unit is either a common electrode voltage or an external bias voltage, not a timing signal.

None of the remaining references appears to cure these deficiencies in *Lee*, as none appears to disclose or suggest any inverter control unit outputting a timing signal according to a control signal from any mode setting unit. Claim 1 is thus patentable over each of the above

references, singly or in combination, for at least the reasons that it recites "an inverter control unit for selectively outputting a timing signal according to the control signal from the mode setting unit." Similarly, claim 4 is patentable for at least the reasons that it recites "an inverter control unit for selectively outputting the timing signal received from the timing controller according to the control signal from the mode setting unit." Likewise, claim 8 as amended is patentable for at least the reasons that it recites "applying the control signal to an inverter control unit from the mode setting unit."

Second, as noted in the latest Office Action, neither *Lee* nor *Yu* teaches or suggests an inverter that can operate in both synchronous and asynchronous mode (Office Action, p. 4). Neither of the remaining references cures this deficiency in *Lee* and *Yu*. In particular, *Nuimura* discloses an inverter 4a that receives a PWM signal Sc, and outputs a driving signal Sd that drives a lamp 4b (¶ [0029]). PWM signal Sc, the input to inverter 4a, is always asynchronous to a separate vertical synchronizing signal Sv (¶ [0035]), while Sd, the output of inverter 4a, is a multiple of Sc (¶ [0029]; FIG. 5). Thus, at most, *Nuimura* only discloses an inverter 4a that operates in a single mode: synchronous to its input Sc. Inverter 4a does not operate in any asynchronous mode. Its input Sc is asynchronous to a different signal Sv, but this does not mean that inverter 4a operates in any asynchronous mode. Rather, it operates synchronously to Sc. The fact that Sc is itself asynchronous to a different signal is irrelevant; inverter 4a still operates in sync with its input.

Park does not appear to cure this deficiency in *Nuimura*, as *Park* does not appear to disclose any inverter that can be operated in both synchronous and asynchronous modes.

Third, as no reference discloses an inverter that can operate in both synchronous and asynchronous modes, no reference can also disclose that this inverter operates in synchronous or asynchronous modes depending on whether a timing signal is received.

Claims 1 and 4 are thus patentable over each of the above references, singly or in combination, for at least the additional reasons that they recite "an inverter which is operated in a synchronous mode upon receiving the timing signal from the inverter control unit, and in an asynchronous mode when the timing signal is not received." Similarly, claim 8 is patentable for at least the additional reasons that it recites "driving a lamp with a voltage applied to the lamp by an inverter, according to an operation mode of the inverter, the operation mode including a synchronous mode and an asynchronous mode" and "a frequency of the voltage applied to the lamp is synchronized with a frequency of the timing signal during the synchronous mode in which the timing signal is output from the inverter control

unit." The remaining pending claims each depend from one of claims 1, 4, or 8, and are thus each also patentable for at least the same reasons as above.

Fourth, under the latest Office Action's interpretation of *Nuimura*, *Nuimura* teaches away from Applicants' claims. The latest Office Action appears to regard the asynchronous input Sc of inverter 4a as an asynchronous mode (e.g., Office Action, p. 4). As above, this is incorrect – inverter 4a may accept an input that is asynchronous with some other signal, but inverter 4a does not itself operate in any asynchronous mode. However, even if the office Action's interpretation of *Nuimura* is correct, *Nuimura* also teaches that signal Sc is as asynchronous with vertical synchronizing signal Sv as possible, in order to minimize the appearance of undesirable lateral stripes on the display screen even when the PWM signal Sc shifts slightly due to, e.g., temperature variations (¶[0035]). That is, if the input Sc is to be considered as an "asynchronous mode" of inverter 4a, then *Nuimura* also teaches that this "asynchronous mode" must be present, or undesirable lateral stripes will occur on the display. Thus, in this interpretation, *Nuimura* would teach against having a synchronous mode, as synchronous modes lead to the display of undesirable lateral stripes. Under the latest Office Action's interpretation of *Nuimura*, *Nuimura* thus teaches directly away from Applicants' recitation of a synchronous mode, and does not form the basis for any valid obviousness rejection. Accordingly, the pending claims would be patentable for this additional reason as well.

CONCLUSION

For the foregoing reasons, Applicant believes that the application is now in condition for allowance. The Director is authorized to charge any deficiency in fees, or credit any overpayment, to Deposit Account No. 50-5029. If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned at (408) 331-1671.

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